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RTL9210B-CG

USB 3.1 GEN2 to PCI EXPRESS GEN3x2/SATA Gen3. BRIDGE

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

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- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2019/12/11	First release.
1.1	2020/06/19	Revised Table 4 Power and Ground, page 7. Revised Table 17 Other Pins, page 11. Revised Table 31 Absolute Maximum Ratings, page 20. Revised Table 32 Recommended Operating Conditions, page 20. Revised Table 33 Electrostatic Discharge Performance, page 21. Corrected minor typing errors.

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1. General Description

The Realtek RTL9210B-CG is a USB (Universal Serial Bus) bridge that combines a USB device with both a PCI Express (PCIe) controller and a SATA controller. Via the PEDET interface of M.2 mechanical, the RTL9210B-CG can auto switch USB-to-PCIe mode, or USB-to-SATA mode.

The RTL9210B-CG supports USB 3.1 GEN2 (Super Speed Plus). It is compatible with USB 3.1 GEN1 (Super Speed), USB High Speed, and Full Speed. It can work normally with auxiliary power. The Mass Storage transaction supports both Bulk Only Transfer (BOT) and USB Attached SCSI Protocol (UASP). For USB, it provides up to 10Gbps bandwidth.

In USB-to-PCIe mode, the RTL9210B-CG supports PCIe Gen3 x2. For PCIe, it provides up to 16Gbps bandwidth. It has full backward compatibility for PCIe Gen2/Gen1 and link width 1 lanes. It supports PCIe 3.0 LTR (Latency Tolerance Reporting). To further reduce power consumption, the RTL9210B-CG supports link power management (PCIe L1. Off and L1. Snooze), PCI MSI (Message Signaled Interrupt) and MSI-X.

In USB-to-PCIe mode, the RTL9210B-CG provides the function of a PCIe host. The PCIe host supports NVM Express, which is an interface that allows a host driver to communicate with an NVMe SSD (Solid-State Disk). The NVMe driver is embedded in customized RAM/Rom/SPI Flash.

In USB-to-SATA mode, the RTL9210B-CG supports SATA host in Gen3 speed. For SATA, it provides up to 6Gbps bandwidth. It has full backward compatibility for SATA Gen2/Gen1.

In USB-to-SATA mode, the RTL9210B-CG provides the function of a SATA host. The SATA host supports AHCI (Advanced Host Controller Interface) which is an interface that allows a host driver to communicate with a SATA HDD (Hard Disk Drive) or SSD. The AHCI driver is embedded in customized RAM/Rom/SPI Flash.

The RTL9210B-CG supports the Type-C connector. It supports a dynamically switching power state with NVMe/SATA/USB power management for power saving mode. It has an algorithm that can balance power consumption and performance.

The RTL9210B-CG is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

General

- USB to PCI Express/SATA bridge
- Integrated with Type-C connector
- Supports External Serial Peripheral Interface (SPI) Flash
- Supports Customized LEDs (includes blinking frequency and duty cycle)
- Supports UART interface
- Supports GPIOs/eFUSE
- Supports I2C interface
- Built-in switching regulator (5V to 1V)
- Built-in LDO (5V to 3.3V)
- Supports 25MHz crystal clock
- 68-pin QFN Green package

USB

- Link bandwidth up to 10Gbps
- Compatible with Full Speed/High Speed/Super Speed/Super Speed Plus
- Supports Bulk Only Transfer (BOT) and USB Attached SCSI (UAS) protocol
- Supports USB link power management
- Supports SCSI command that translation to NVM Express

Type-C

- Supports Cable Orientation Detection

PCI Express

- Link speed up to 8GT/s
- Link width up to 2 lanes
- Being compatible with PCI Express Gen1/Gen2/Gen3
- Maximum bandwidth up to 16GT/s
- Supports LTR (Latency Tolerance Reporting)
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports PCIe link power management, ASPM L1, CLKREQ, and L1 substate

NVM Express

- Supports standard command set
- Dynamic power state translation
- Strong Error handing and recovery
- Supports all command set of NVM Express SCSI Translation (e.g., Unmap, Security protocol in/out …)
- Supports Security Send and Receive
- Supports SMART/Health information

SATA

- Link speed up to 6GT/s
- Compatible with SATA Gen1/Gen2/Gen3
- Supports SATA link power management. Partial mode/Slumber mode/DEVSLP mode.

AHCI

- Supports standard command set
- Dynamic power state translation
- Strong Error handling and recovery
- Supports full command set of SATA SCSI Translation (e.g., Unmap, Security protocol in/out …)
- Supports Security Send and Receive
- Supports SMART/Health information

3. System Applications

- USB3.1 SS+/SS/HS with both PCIE and SATA SSD mass storage on motherboard, notebook, Embedded or mobile phone system supporting BOT and UASP mass storage specifications.

4. Block Diagram

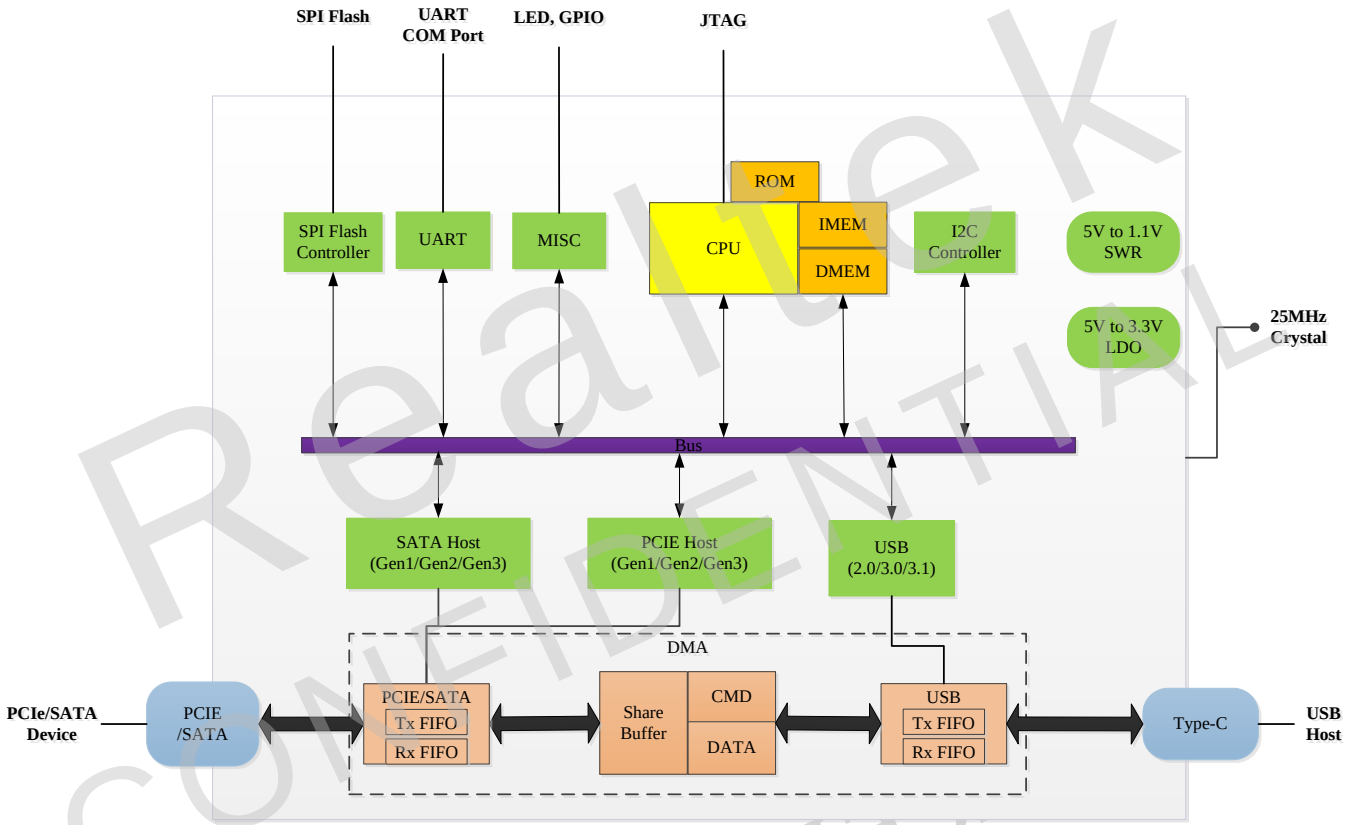


Figure 1. Block Diagram

5. Pin Assignments

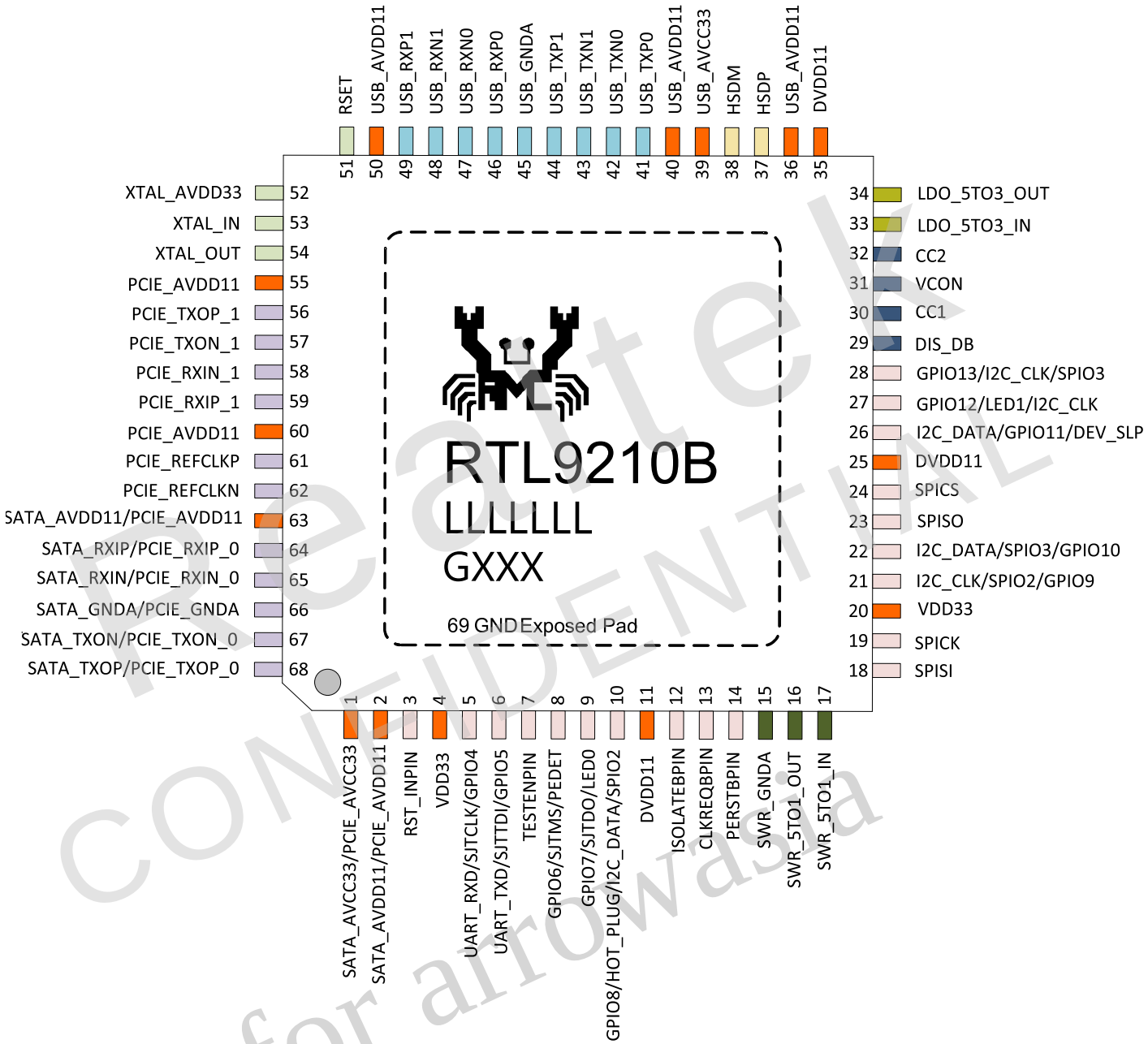


Figure 2. RTL9210B-CG Pin Assignments

6. Pin Descriptions

The signal type codes below are used in the following tables:

I:	Input	S/T/S:	Sustained Tri-State
O:	Output	O/D:	Open Drain
T/S:	Tri-State Bi-Directional Input/Output Pin	P:	Power
G:	GND		

6.1. General Pins

6.1.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
ISOLATEBPIN	O	12	Isolate Pin: (Active Low, 3.3V output). The RTL9210B-CG uses the ISOLATEBPIN to control the PCIE device main power circuit in USB-to-PCIE mode. For USB-to-SATA mode, this pin is used to control SATA power.

6.1.2. Clock

Table 2. Clock

Symbol	Type	Pin No	Description
XTAL_AVDD33	PI	52	3.3V power for Clock Source.
XTAL_IN	I	53	Input of 25MHz Clock Reference.
XTAL_OUT	IO	54	Input of External Clock Source. Output of 25MHz Clock Reference.

6.1.3. Regulator and Reference

Table 3. Regulator and Reference

Symbol	Type	Pin No	Description
LDO_5TO3_OUT	P/O	34	Linear Regulator (LDO) 3.3V Output. *Note: The embedded LDO is designed for RTL9210B-CG internal use only. Do not provide this power source to other devices.*
LDO_5TO3_IN	P/I	33	Linear Regulator (LDO) 5V Input.
SWR_5TO1_OUT	P/O	16	Switching Regulator (SWR) 1.1V Output. *Note: The embedded SWR is designed for RTL9210B-CG internal use only. Do not provide this power source to other devices.*
SWR_5TO1_IN	P/I	17	Switching Regulator (SWR) 5V Input.
RSET	I	51	Reference (External resistor reference).

6.1.4. Power and Ground

Table 4. Power and Ground

Symbol	Type	Pin No	Description
PCIE_AVCC33	P	1	PCIE Analog 3.3V Power Supply.
PCIE_AVDD11	P	2,55,60,63	PCIE Digital 1.1V Power Supply.
SATA_AVCC33	P	1	SATA Analog 3.3V Power Supply.
SATA_AVDD11	P	2,63	SATA Digital 1.1V Power Supply.
USB_AVCC33	P	39	USB Analog 3.3V Power Supply.
USB_AVDD11	P	36,40,50	USB Digital 1.1V Power Supply.
VDD33	P	4,20	Digital 3.3V Power Supply.
DVDD11	P	11,25,35	Digital 1.1V Power Supply.
SWR_GNDA	G	15	SWR Ground.
USB_GNDA	G	45	USB Ground.
PCIE_GNDA	G	66	PCIE Ground.
SATA_GNDA	G	66	SATA Ground.
GND	G	69	Ground (Exposed Pad).

Note: Refer to the latest schematic circuit for correct configuration.

6.1.5. Mode Selection Pin

Table 5. Mode Selection Pin

Symbol	Type	Pin No	Description
PEDET	I	8	Switch USB-to-SATA / USB-to-PCIE MODE. 1: PCIE MODE 0: SATA MODE

6.2. Peripheral Pins

6.2.1. USB Interface Pins

Table 6. USB Interface Pins

Symbol	Type	Pin No	Description
USB_TXP0	O	41	USB SS/SS+ Transmit Differential Pair0.
USB_TXN0	O	42	
USB_TXP1	O	44	USB SS/SS+ Transmit Differential Pair1.
USB_TXN1	O	43	
USB_RXP0	I	46	USB SS/SS+ Receive Differential Pair0.
USB_RXN0	I	47	
USB_RXP1	I	49	USB SS/SS+ Receive Differential Pair1.
USB_RXN1	I	48	
HSDP	IO	37	USB 2.0/USB 1.1 Differential Signal Pair.
HSDM	IO	38	

6.2.2. Type-C Interface

Table 7. Type-C Interface

Symbol	Type	Pin No	Description
DIS_DB	I	29	Dead battery function configuration pin. Connect this pin to GND to disable dead battery 'Rd'. Leave this pin floating to enable dead battery 'Rd'.
CC1	IO	30	Type-C configuration channel and Data I/O.
CC2	IO	32	Type-C configuration channel and Data I/O.
VCON	PI	31	5V power input for internal VCONN switches.

6.2.3. SPI (Serial Peripheral Interface) Flash Pins

Table 8. SPI (Serial Peripheral Interface) Flash Pins

Symbol	Type	Pin No	Description
SPICS	O	24	SPI Flash Chip Select.
SPICLK	O	19	SPI Flash Serial Data Clock.
SPISI	IO	18	Serial Data Input (for 1x flash). Serial Data Input/output (for 2x/4x flash).
SPISO	IO	23	Serial Data Output (for 1x flash). Serial Data Input/output (for 2x/4x flash).
SPISO2	IO	21	Serial Data Input/output (for 4x flash). *Note: This is a share-pin with I2C_CLK/GPIO9.*
SPISO3	IO	22	Serial Data Input/output (for 4x flash). *Note: This is a share-pin with I2C_DATA/GPIO10.*

6.2.4. I2C Interface

Table 9. I2C Interface

Symbol	Type	Pin No	Description
I2C_CLK	O	21	I2C clock. *Note: This is a share-pin with SPISO2/GPIO9.*
I2C_DATA	IO	22	I2C data. *Note: This is a share-pin with SPISO3/GPIO10.*

Note: Only Master mode is supported.

6.2.5. UART Interface

Table 10. UART Interface

Symbol	Type	Pin No	Description
UART_RXD	I	5	UART interface Data In. *Note: This is a share-pin with SJCLK/GPIO4.*
UART_TXD	O	6	UART interface Data Out. *Note: This is a share-pin with SJTDI/GPIO5.*

6.2.6. JTAG Interface

Table 11. JTAG Interface

Symbol	Type	Pin No	Description
SJTDO	O	9	Test Data Out. *Note: This is a share-pin with GPIO7/LED0.*
SJTMS	I	8	Test Mode Select. *Note: This is a share-pin with GPIO6.*
SJTDI	I	6	Test Data In. *Note: This is a share-pin with UART_TXD/GPIO5.*
SJTCLK	I	5	Test Clock. *Note: This is a share-pin with UART_RXD/GPIO4.*

6.2.7. LEDs

Table 12. LEDs

Symbol	Type	Pin No	Description
LED0	O	9	LED Pin. *Note: This is a share-pin with GPIO7/SJTDO.*
LED1	O	27	LED Pin. *Note: This is a share-pin with GPIO12/I2C_CLK.*

Note: Refer to the latest schematic circuit for correct configuration.

6.2.8. GPIO Pins

Table 13. GPIO Pins

Symbol	Type	Pin No	Description
GPIO4	IO	5	General Purpose Input / Output Pin (3.3V Input/Output). *Note: This is a share-pin with UART_RXD/SJTCLK.*
GPIO5	IO	6	General Purpose Input / Output Pin (3.3V Input/Output). *Note: This is a share-pin with UART_TXD/SJTDI.*
GPIO6	IO	8	General Purpose Input / Output Pin. *Note: This is a share-pin with SJTMS/PEDET.*
GPIO7	IO	9	General Purpose Input / Output Pin. *Note: This is a share-pin with SJTDO/LED0.*
GPIO8	IO	10	General Purpose Input / Output Pin. *Note: This is a share-pin with SJTDO2/HOT_PLUG/I2C_DATA/SPIO2.*
GPIO9	IO	21	General Purpose Input / Output Pin. *Note: This is a share-pin with I2C_CLK/SPISIO2.*
GPIO10	IO	22	General Purpose Input / Output Pin. *Note: This is a share-pin with I2C_DATA/SPISIO3.*
GPIO11	IO	26	General Purpose Input / Output Pin. *Note: This is a share-pin with I2C_DATA.*

Symbol	Type	Pin No	Description
GPIO12	IO	27	General Purpose Input / Output Pin. *Note: This is a share-pin with LED1/I2C_CLK.*
GPIO13	IO	28	General Purpose Input / Output Pin. *Note: This is a share-pin with LED1/I2C_CLK/SPIO3.*

6.3. PCIE Mode Pins

6.3.1. PCI Express Interface

Table 14. PCIe Interface

Symbol	Type	Pin No	Description
PCIE_REFCLKP	O	61	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
PCIE_REFCLKN	O	62	
PCIE_RXIP_0	I	64	PCI Express Receive Differential Pair 0.
PCIE_RXIN_0	I	65	
PCIE_TXOP_0	O	68	PCI Express Transmit Differential Pair 0.
PCIE_TXON_0	O	67	
PCIE_RXIP_1	I	59	PCI Express Receive Differential Pair 1.
PCIE_RXIN_1	I	58	
PCIE_TXOP_1	O	56	PCI Express Transmit Differential Pair 1.
PCIE_TXON_1	O	57	
PERSTBPIN	O	14	PCI Express Reset Signal: (Active Low, 3.3V output). When the PERSTB is asserted at power-on state, the PCIE device returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	I/O/D	13	Reference Clock Request Signal (Open Drain; Active Low, 3.3V compatible output mode with a weak external pull up resistor). This signal is used by the PCIE device to request starting of the PCI Express reference clock. The signal is also used by the L1 substate mechanism. In this case, CLKREQB can be asserted by the RTL9210B-CG to initiate an L1 exit.

6.3.2. PCIe Hot Plug Pin

Table 15. PCIe Hot Plug Pin

Symbol	Type	Pin No	Description
HOT PLUG PIN	I	10	PCIe hot plug pin.

6.4. SATA Mode Pins

6.4.1. SATA Interface

Table 16. SATA Interface

Symbol	Type	Pin No	Description
SATA_RXIP	I	64	SATA Receive Differential Pair 0.
SATA _RXIN	I	65	
SATA _TXOP	O	68	SATA Transmit Differential Pair 0.
SATA _TXON	O	67	
DEV_SLP	O	26	SATA device sleep mode pin. *Note: This is a share-pin with GPIO11.*

6.5. Other Pins

Table 17. Other Pins

Symbol	Type	Pin No	Description
TESTEN	I	7	Enable TEST mode. 1: Enable. Enable JTAG debug function 0: Disable
RST_INPIN	I	3	Reset pin. Low reset.

6.6. Share-Pin Default Function

Table 18. Share Pin Default Function

Share-Pin No	Type	Default Function	Description
5	I	UART_RXD	UART interface Data In.
6	O	UART_TXD	UART interface Data Out.
8	IO	GPIO6	General Purpose Input / Output Pin.
9	IO	GPIO7	General Purpose Input / Output Pin.
10	IO	GPIO8	General Purpose Input / Output Pin.
21	O	I2C_CLK	I2C clock.
22	IO	I2C_DATA	I2C data.
26	IO	GPIO11	General Purpose Input / Output Pin.
27	IO	GPIO12	General Purpose Input / Output Pin.
28	IO	GPIO13	General Purpose Input / Output Pin.

7. Functional Description

7.1. USB Bus Interface

The SIE (Serial Interface Engine) employs a robust hardwired USB protocol implementation so that the entire USB interface operation can be done without firmware intervention.

USB Super speed plus (USB3.1 Gen2) extends the performance range by doubling the SuperSpeed USB clock rate to 10Gbps and enhancing data encoding efficiency.

For bulk transaction (Bulk-in, Bulk-out, and SuperSpeed (Plus) bulk streaming protocol), appropriate responses and handshake signals are generated by the SIE. The SIE analog transceiver is compatible with driver and receiver characteristics defined in USB Specification Rev. 3.1.

7.1.1. USB Interface

The RTL9210B-CG supports two types of Mass storage interface: UASP and BOT. Both UASP & BOT run standard drivers without installing additional vendor specific drivers. For the UASP interface, the RTL9210B-CG supports four Bulk endpoints, two for mass storage data transfer, two for information transfer. For the BOT interface, the RTL9210B-CG supports two Bulk endpoints, data and information transfer share the same endpoint.

7.1.2. Endpoint 0

All USB devices support a common access mechanism for accessing information through this control pipe. Associated with the control pipe at endpoint 0 is the information required to fully describe the USB device.

7.1.3. Endpoint Bulk-In

The RTL9210B-CG transfers mass storage data to the host via this endpoint. The maximum Bulk-In packet size is 1024 bytes. If the mass storage data is larger than 1024 bytes, the RTL9210B-CG splits the data into multiple USB packets.

7.1.4. Endpoint Bulk-Out

The host sends mass storage data to the RTL9210B-CG via this endpoint. The maximum Bulk-Out packet size is 1024 bytes. If the data length is larger than 1024 bytes, the host will send the data in multiple USB packets.

7.1.5. Streaming Bulk-In/Out protocol

The RTL9210B-CG supports multiple stream mode for UASP protocol. The host and device manage the Endpoint buffers via ‘StreamID’. The RTL9210B-CG also supports out-of-order data transfers required for mass storage device command queuing.

The host can burst multiple streaming packets to the device. When the device has data available for a specific stream, it issues ERDY with the specific ‘StreamID’ to host. The host then selects endpoint buffers with the ‘StreamID’ and starts the data transfer.

7.2. PCI Express

The RTL9210B-CG is compatible with PCI Express Base Specification Revision 3.0, and runs at a 8GHz signaling rate on each lane with X2 link width, i.e., one transmit and one receive differential pair. The RTL9210B-CG supports three types of PCI Express messages:

- Interrupt messages
- Error messages
- Power management messages

PCI Express lane polarity reversal and link reversal are also supported to ease PCB layout constraints.

The RTL9210B-CG supports Max link speed 8.0 GT/s and is compatible with 2.5 GT/s and 5.0 GT/s. For backwards compatibility, the link will first train to L0 with 2.5 GT/s, which uses 8b/10b encoding data rate. When a PCI Express Link is operating at a data rate of 8.0 GT/s it uses 128b/130b encoding.

7.2.1. Standard Capability Support

Table 19. Standard Capability Support

Capability ID	Description
01h	PCI Power Management Interface
10h	PCI Express
11h	MSI-X

7.2.2. Extended Capability Support

Table 20. Extended Capability Support

Capability ID	Description
0018h	Latency Tolerance Reporting (LTR)
001Eh	L1 PM Substates

7.2.3. Link Capability & Device Control

Table 21. Link Capability & Device Control

Capability	Description
Maximum Link Width	2 lane support
Max Link Speed	8GT/s
Max bandwidth	16GT/s (8GT/s x2)

7.2.4. Active State Power Management (ASPM)

The RTL9210B-CG supports PCI Express ASPM in the following states:

- L0 – Active state
- L0s – power saving state, quick entry and exit latency
- L1 – lower power saving state, higher entry and exit latency
- L1 + CLKREQ# – low power state, Rx/Tx off, PLL off
- L1 substate – L1.1 & L1.2 low power mode

7.2.5. Hot-Plug

The RTL9210B-CG supports Hot-plug function with SW solution. It is compatible with CF express.

7.3. SCSI Protocol

7.3.1. SCSI Command List

Table 22. SCSI Command List

SCSI Command	Op Code	Data Type
FORMAT UNIT	0x04	Data Out
INQUIRY	0x12	Data In
LOG SENSE	0x4D	Data In
MODE SELECT(6)	0x15	Data Out
MODE SELECT(10)	0x55	Data Out
MODE SENSE(6)	0x1A	Data In
MODE SENSE(10)	0x5A	Data In
Read(6)	0x08	Data In
Read(10)	0x28	Data In
Read(12)	0xA8	Data In
Read(16)	0x88	Data In
READ CAPACITY(10)	0x25	Data In
READ CAPACITY(16)	0x9E	Data In
REQUEST SENSE	0x03	Data In
START STOP UNIT	0x1B	N/A
SYNCHRONIZE CACHE(10)	0x35	N/A
SYNCHRONIZE CACHE(16)	0x91	N/A
TEST UNIT READY	0x0	N/A
UNMAP	0x42	Data Out
WRITE(6)	0x0A	Data Out
WRITE(10)	0x2A	Data Out
WRITE(12)	0xAA	Data Out
WRITE(16)	0x8A	Data Out
WRITE BUFFER	-	Data Out

7.4. NVM Express

The RTL9210B-CG is compatible with NVM Express Specification Revision 1.3, which allows a PCI Express host to communicate with a non-volatile memory subsystem. NVM Express is an interface of PCIe host controller, it provides command submission and completion paths. It can support multi I/O queues and parallel operation.

The RTL9210B-CG is also compatible with NVM Express: SCSI Translation Reference, which allows SCSI over NVMe translation.

7.4.1. Admin Command

Table 23. Admin Commands

Admin Commands	OP Code
Delete I/O Submission Queue	00h
Create I/O Submission Queue	01h
Get Log Page	02h
Delete I/O Completion Queue	04h
Create I/O Completion Queue	05h
Identify	06h
Abort	08h
Set Features	09h
Get Features	0Ah
Asynchronous Event Request	0Ch
Device Self-test	14h
Security Send	81h
Security Receive	82h

7.4.2. NVM Commands Set

Table 24. NVM Commands Set

NVM Commands	OP Code
Flush	00h
Write	01h
Read	02h
Write uncorrectable	04h
Compare	05h
Write zeros	08h
Dataset Management	09h

7.4.3. Power Control

The RTL9210B-CG supports auto power state change for power saving. An algorithm sets the SSD device in the ideal power state for outstanding power saving, without reduced performance.

7.5. SATA

The RTL9210B-CG integrates a Serial ATA AHCI host controller that provides an interface between a host and device. This interface is a peer-to-peer connection and the data is transmitted or received from one Serial ATA compatible device. It is designed to meet the Serial ATA 3.0 standard, and runs at a 6GHz signaling rate.

The RTL9210B-CG supports Max link speed 6.0 Gb/s and is compatible with 1.5 Gb/s and 3.0 Gb/s.

7.5.1. Features

- The Host controller is compatible with the SATA III extension specification
  - Supports serial-ATA 3.1 Spec
  - Supports SATA III (1.5G/3G/6G) Spec
  - Supports SATA AHCI 1.31 Spec (first-party DMA)
  - Supports PIO transfer
  - Supports NCQ (Native Command Queuing)
  - Supports Power management including automatic partial-to-slumber transition
- PHY Layer (analog) function module is compatible with 1.0a Specification
  - Supports Out-of-Band signal generator and detector
  - Supports speed transition between 1.5Gbps and 3Gbps and 6Gbps
  - Supports Low Power Mode (Partial, Slumber, Device sleep)
- Device status detection and auto speed negotiation
- Supports low power mode

7.6. AHCI

The RTL9210B-CG is compatible with AHCI Revision 1.3.1, which allows a SATA host to communicate with a non-volatile memory subsystem.

The RTL9210B-CG also is compatible with SCSI/ATA Translation Reference, which allows a SCSI over ATA command translation.

7.7. SPI (Serial Peripheral Interface) Flash

SPI Flash is enabled by the RTL9210B-CG through the Chip Select pin, and accessed via a 5-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), Serial Data Output2 (SO2), Serial Data Output 3 (SO3) and Serial Clock (SCK). The RTL9210B-CG supports up to x 4 SPI flash and is compatible with x 1/x 2. The SPI flash utilizes an 8-bit instruction register. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Compared to a parallel bus interface, the Serial Peripheral Interface provides simpler wiring and much less interaction (crosstalk) among the conductors in the cable. This minimizes the number of conductors, pins, and the IC package size, reducing the cost of making, assembling, and testing the electronics.

Note 1: SPI Flash size (firmware size) is based on features and customizable functions. For the exact flash size, contact Realtek FAE or your Realtek Agent.
Note 2: SPI Flash frequency default supports 62.5 MHz clock. If the SPI flash frequency is lower than 62.5MHz, contact Realtek FAE or your Realtek Agent.

Table 25. SPI Flash Interface

SPI Flash	Description
SPISO	Output Data Bus.
SPISI	Input Data Bus.
SPISK	SPI Flash Serial Data Clock.
SPICSB	SPI Flash Chip Select.
SPISO2	Input/output Data Bus (4x flash).
SPISO3	Input/output Data Bus (4x flash).

7.8. Customizable LED Configuration

The RTL9210B-CG supports customizable LED operation modes via control registers 64h. An individual control register of each LED and a global feature control register are provided to support customized LED signals, which are described in Table 26 & Table 27.

Table 26. Customized LEDs

LEDSEL	Interface	LINK						Active	High/Low Active
-	USB/SATA or PCIe	All_Speed	USB20 PCIe/SATA gen1	USB30 PCIe/SATA gen2	USB30 PCIe/SATA gen3	*USB x 2 PCIe x 2	Power On	-	-
LED 0	Bit 1	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 14	Bit 15

Note that bit 7 will be RVD (Reserved) in USB-to-SATA Mode.

Table 27. LED Feature Control Description

Feature Control	Description
High/Low Active	1: LED Low Active; 0: LED High Active
Interface USB or PCIe/SATA	1: PCIe/SATA; 0: USB
LINK x2	LED lit if link on by 2 lanes.
Active	LED blinks when interface has transport or receive data.
LINK	LED lit if device link on configuration speed.

The RTL9210B-CG LED register default values are shown in Table 28.

Table 28. LED Register Default Value

LEDSEL	Interface	LINK						Active	High/Low Active
-	USB or PCIe/ SATA	All_ Speed	USB20 PCIe/SATA gen1	USB30 PCIe/SATA gen2	USB30 PCIe/SATA gen3	USB x 2 PCIe x 2	Power On	-	-
LED 0	0	0	0	0	0	0	1	1	0

When implementing customized LED:

Configure MISC register address offset 0x64 to support your own LED signals. For examples, if the value is configured as C010h (1100000000010000b), the LED action is lit when USB link on 30, with no blink.

7.8.1. LED Blinking Frequency Control

The RTL9210B-CG supports LED blinking frequency control via MISC address 68h to control the user's LED blinking frequency and duty cycle. If the b_freq[1:0] set as 0x3 and the b_duty_cycle[1:0] set as 0x3, the LED blinking frequency is 80ms and the duty cycle is 75%.

Table 29. LED Blinking Frequency Control (MISC Register Offset 0x68)

Bit	RW	Description
b_freq[1:0]	RW	LED Blinking Frequency. 0: 320ms 1: 240ms 2: 160ms (Default) 3:80ms
b_duty_cycle[1:0]	RW	LED Blinking Duty Cycle. 0: 12.5% 1: 25% 2: 50% (Default) 3: 75%

7.9. Power Management

The RTL9210B-CG is compatible with ACPI such as to support an Operating System-directed Power Management (OSPM) environment.

7.10. USB Link Power Management

The RTL9210B-CG supports full USB Link Power Management (LPM). It provides an efficient way for the host to manage power consumption.

- For USB 2.0, the RTL9210B-CG supports L0/L1/Suspend (L2) mode
- For USB 3.1, the RTL9210B-CG supports U1/U2/Suspend (U3) mode

UTMI clock & PCLK clock are disabled while in Suspend mode.

If USB host and hub support LPM, the host and hub can put the device into a low power state. The RTL9210B-CG will deactivate some of its circuits to reduce power consumption in the low power state, and go back to full power functionally in active state.

7.11. PCI Express L1.1 and L1.2

The RTL9210B-CG supports PCIe L1substate L1.1 and L1.2 power management features. L1+CLKREQ# stops (or provides) the REFCLK to a device by toggling the CLKREQB pin to enter L1.1 and L1.2 states (saving more power than L1+CLKREQ# only). Table 30 shows the PCIe Port Circuit On/Off states.

Table 30. L1.Off and L1.Snooze PCIe Port Circuit On/Off

State	PLL	Common Mode Keeper	RX/TX
L1	On	On	Off / Idle
L1+CLKREQ#	Off	On	Off / Idle
L1.1	Off	On	Off
L1.2	Off	Off	Off

7.12. SATA Power Management

The RTL9210B-CG supports full SATA power management. Partial, slumber, and device sleep all can be realized by SW.

7.13. Mode Switching

The RTL9210B-CG supports a bus controller that can switch between PCIE and SATA determined by the PEDET pin (share-pin with SJTMS/GPIO6 pin). Relative description has been shown in 6.1.5.

8. Characteristics

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 31. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
LDO_5TO3_IN, SWR_5TO1_IN, VCON	Supply Voltage 5V	-0.3	5.5	V
VDD33, USB_AVCC33, PCIE_AVCC33, SATA_AVCC33	Supply Voltage 3.3V	-0.3	3.6	V
DVDD11, USB_AVDD11, PCIE_AVDD11, SATA_AVDD11	Supply Voltage 1.1V	-0.3	1.2	V
3.3V DCinput 3.3V DCoutput	Input Voltage Output Voltage	-0.3	3.6	V
1.1V DCinput 1.1V DCoutput	Input Voltage Output Voltage	-0.3	1.2	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.2. Recommended Operating Conditions

Table 32. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	LDO_5TO3_IN, SWR_5TO1_IN VCON	4.5	5	5.5	V
	VDD33, USB_AVCC33, PCIE_AVCC33, SATA_AVCC33	3.14	3.3	3.46	V
	DVDD11, USB_AVDD11, PCIE_AVDD11, SATA_AVDD11	1.045	1.1	1.155	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note1: Refer to the most updated schematic circuit for correct configuration.
Note 2: Internal voltage 3.3V and 1.1V cannot be adjusted.

8.3. Electrostatic Discharge Performance

Table 33. Electrostatic Discharge Performance

Test Item	Results
HBM ESD	All Pins: 3.5 KV
MM ESD	All Pins: 100V
CDM ESD	All Pins: 1.5KV
Latch Up	I/O Pins: 100mA Power Pins: 1.5x VDD

8.4. Crystal Requirements

Table 34. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
F_{ref} System	Parallel Resonant Crystal Frequency Tolerance, On Board.	-80	-	+80	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
Jitter	Broadband Peak-to-Peak Jitter[2].	-	-	200	ps
DL	Drive Level.	-	-	0.3	mW

Note 1: Jitter measurement result can be confirmed after the Crystal component specification and board layout are reviewed by Realtek.
Note 2: C_{load} should be verified by the Crystal vendor.

8.5. Oscillator Requirements

Table 35. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25	-	MHz
Frequency Stability	T_a = 0°C~70°C	-30	-	+30	ppm
Frequency Tolerance	T_a = 25°C	-50	-	+50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[2]	-	-	-	200	ps
V_{ih}	-	1.4	-	-	V
V_{il}	-	-	-	0.4	V
Rise Time	-	-	-	10	ns
Fall Time	-	-	-	10	ns
Operation Temp Range	-	0	-	70	°C

Note 1: The CLK source can come from other places in the system, but it must accord with the parameters above.
Note 2: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps. If the items listed below are tested and confirmed by Realtek, this can be modified to Broadband RMS=9ps; 25KHz to25MHz RMS=3.5ps.
Test Items: 1. SNR, 2. Power Ripple, 3. RSET Ripple, 4. IEEE Gigabit Waveform, 5. Bit Error Rate Test.

8.6. Environmental Characteristics

Table 36. Environmental Characteristics

Parameter	Range	Units
Storage Temperature	-55 ~ +125	°C
Ambient Operating Temperature	0 ~ 70	°C
Moisture Sensitivity Level (MSL)	Level 3	N/A

8.7. DC Characteristics

Table 37. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
LDO_5TO3_IN, SWR_5TO1_IN VCON	5V Supply Mean Voltage	-	4.5	5	5.5	V
PCIE_AVDD33 VDD33 USB_AVDD33 SATA_AVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
PCIE_AVDD11 DVDD11 USB_AVDD11 SATA_AVDD11	1.1V Supply Mean Voltage	-	1.045	1.1	1.155	V
Voh	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9*VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	I_{ol} = 4mA	0	-	0.1*VDD33	V
Vih	Minimum High Level Input Voltage for 3.3V	-	2	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	Vin = VDD33 or GND	0	-	0.5	µA
Icc33	Average Operating Supply Current from 3.3V	U3.1 gen2 / PCIe 3.0 with heavy DATA transmit	-	-	-	mA
Icc11	Average Operating Supply Current from 1.1V	USB3.1 gen2 / PCIe 3.0 with heavy DATA transmit	-	-	-	mA
Isys5	Average Operating Supply Current for total system 5V (includes 3.3/1.1V power consumption)	U3 gen2 / PCIe 3.0 with heavy DATA transmit	-	-	-	mA

Note 1: Refer to the latest schematic circuit for correct configuration.
Note 2: All Supply Mean Voltage power noise <±5% of Mean Voltage.
*Note 3: The total operating current Isys5=Icc33+((Icc11*1.1)/ SWR_efficiency / 5), where SWR_efficiency=0.75 for SWR-mode.*
Note 4: Internal voltage 3.3V and 1.1V cannot be adjusted.

8.8. Reflow Profile Recommendations

Table 38. Reflow Profile Recommendations

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Minimum Preheat Temperature (T_{smin})	100°C	150°C
Maximum Preheat Temperature (T_{smax})	150°C	200°C
Preheat Time (t_S) from T_{smin} to T_{smax}	60~120 seconds	60~120 seconds
Ramp-Up Rate (T_L to T_p)	3°C/second max.	3°C/second max.
Liquidus Temperature (T_L)	183°C	217°C
Time (t_L) Maintained above T_L	60~150 seconds	60~150 seconds
Peak Package Body Temperature (T_p)	235°C	260°C
Time $(t_p)^2$ within 5°C of Peak T_P	20 seconds	20 seconds
Ramp-Down Rate (T_p to T_L)	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature (T_p)	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the topside of the package, measured on the package body surface.
Note 2: Tolerance for Tp is defined as a supplier's minimum and a user's maximum.
Note 3: Reference document: IPC/JEDEC J-STD-020D.1.

8.9. AC Characteristics

8.9.1. SPI Flash

8.9.1.1 SPI Flash Commands

Table 39. SPI Flash Commands

Command	Operation Code	Action
WREN	06h	Write Enable
WRDI	04h	Write Disable
RDID	9Fh	Read Manufacturer and Product ID
RDSR	05h	Read Status Register
WRSR	01h	Write Status Register
Read	03h	Read
Page Program	02h	Page Program
Sector Erase (4K)	20h	Erase The Selected Sector
Block Erase (64K)	D8h	Erase The Selected Block
Chip Erase	60h or C7h	Erase Whole Chip

8.9.1.2 SPI Flash Command Sequence

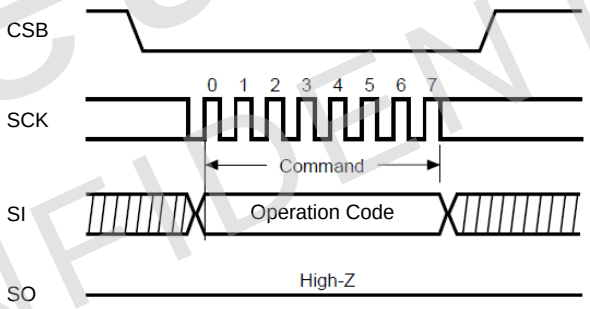


Figure 3. WREN/WRDI Command Sequence

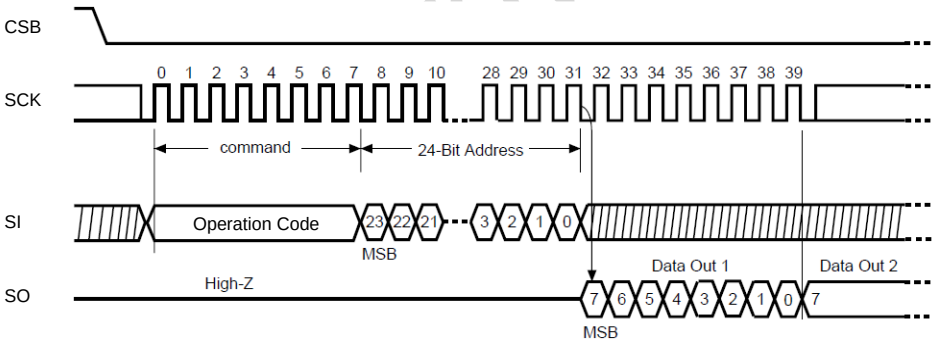


Figure 4. Read Command Sequence

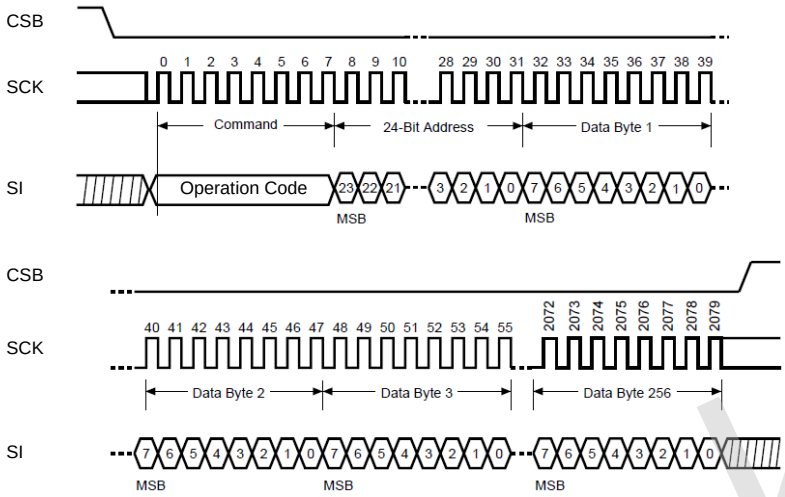


Figure 5. Page Program Command Sequence

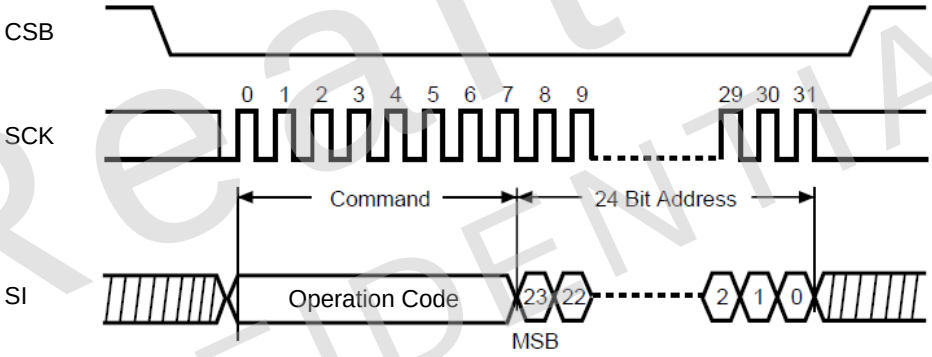


Figure 6. Sector/Block Erase Command Sequence

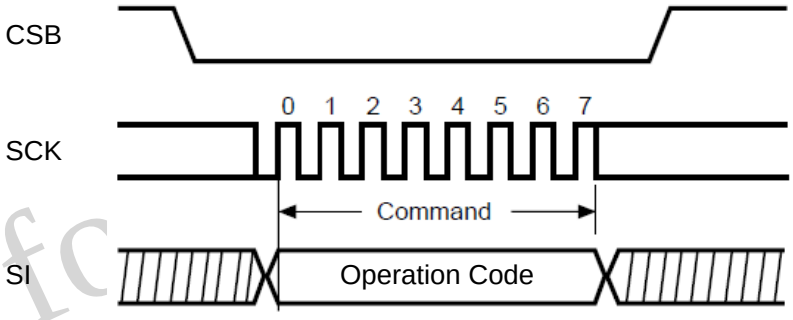


Figure 7. Chip Erase Command Sequence

8.9.2. SPI Flash Interface Timing

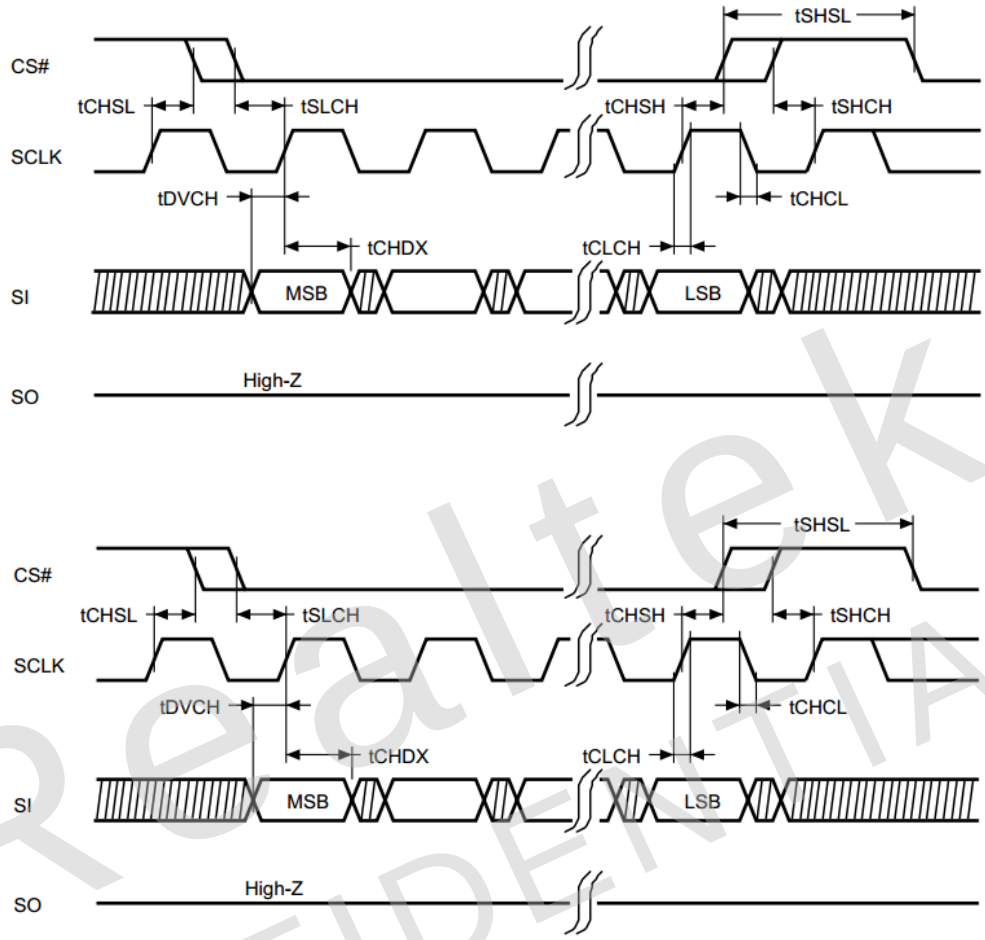


Figure 8. SPI Flash Interface Timing

Table 40. SPI Flash Access Timing Parameters

Symbol	Parameter	Min	Typical	Max	Unit
fSCK	Clock Frequency controller can provide	62.5	-	-	MHz
tCH	Clock High Time	500/fSCK	-	-	ns
tCL	Clock Low Time	500/fSCK	-	-	ns
tCLCH	Clock Rise Time	0.1	-	-	V/ns
tCHCL	Clock Fall Time	0.1	-	-	V/ns
tDVCH	SI Setup Time(SI Valid to Clock High)	125/fSCK	-	-	ns
tCHDX	SI Hold Time(Clock High to SI invalid)	375/fSCK	-	-	ns
tSHQZ	SO Disable Time	-	-	-	ns
tCLQV	Clock Low to SO Valid	-	-	500/fSCK	ns
tCLQX	Output Hold Time	-	-	-	ns
tSOCH	SO Setup Time(SO Valid to Clock High)	0	-	-	ns
tSODX	SO Hold Time(Clock High to SO Invalid)	0	-	-	ns

8.10. PCI Express Bus Parameters

8.10.1. Data Rate Dependent Transmitter Parameters

Table 41. Data Rate Dependent Transmitter Parameters

Symbol	Parameter Description	2.5 GT/s	5.0 GT/s	8.0 GT/s	Units	Notes
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.0375 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm. Does not include SSC variations.
BWTX-PKG-PLL1	Tx PLL bandwidth corresponding to $PKG_{TX-PLL1}$	1.5 (min), 22.0 (max)	8.0 (min), 16.0 (max)	2.0 (min), 4.0 (max),	MHz	Second order PLL jitter transfer bounding function. Notes 1, 2.
BWTX-PKG-PLL2	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$	N/A	5.0 (min), 16.0 (max)	2.0 (min) 5.0 (max)	MHz	2.5 GT/s specifies only one combination of PLL BW and jitter. Notes 1, 2.
PKGTX-PLL1	Tx PLL peaking corresponding to $BW_{TX-PKG-PLL1}$	3.0 (max)	3.0 (max)	2.0 (max)	dB	Second order PLL jitter transfer bounding function. Notes 1, 2.
PKG-TX-PLL2	Tx PLL peaking corresponding to $BW_{TX-PKG-PLL2}$	N/A	1.0 (min)	1.0 (max)	dB	2.5 GT/s specifies only one combination of PLL BW and jitter. Notes 1, 2.
VTX-DIFF-PP	Differential peak-peak Tx voltage swing for full swing operation	800-1200	800-1200	800-1300	mVPP	As measured with compliance test load. Defined as 2*|VTXD+ - VbTXD-|. Note 3.
VTX-DIFF-PP-LOW	Differential peak-peak Tx voltage swing for low swing operation	400 (min)-1200 (max)	400-1200	400 (min)-1300(max)	mVPP	As measured with compliance test load. Defined as 2*|VTXD+ - VbTXD-|. Note 3.
VTX-EIEOS-FS	Minimum voltage swing during EIEOS for full swing signaling	N/A	N/A	250 (min)	mVPP	Note 4.
VTX-EIEOS-RS	Minimum voltage swing during EIEOS for reduces swing signaling	N/A	N/A	232 (min)	mVPP	Note 4.

Symbol	Parameter Description	2.5 GT/s	5.0 GT/s	8.0 GT/s	Units	Notes
$ps21_{TX-ROOT-DEVICE}$	Pseudo package loss of a device containing root ports	N/A	N/A	3.0 (max)	dB	Note 5.
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss for all devices not containing root ports	N/A	N/A	3.0 (max)	dB	Note 5.
VTX-BOOST-FS	Maximum nominal Tx boost ratio for full swing	N/A	N/A	8.0	dB	Nominal boost beyond 8.0 dB is limited to guarantee that ps21TX limits are satisfied.
VTX-BOOST-RS	Maximum nominal Tx boost ratio for reduced swing	N/A	N/A	2.5	dB	Assumes ±1.0 dB tolerance.
EQTX-COEFF-RES	Tx coefficient resolution	N/A	N/A	1/63 (min) 1/24 (max)	N/A	-
VTX-DE-RATIO-3.5dB	Tx de-emphasis ratio for 2.5 and 5.0 GT/s	2.5 (min) 4.5 (max)	2.5 (min) 4.5 (max)	N/A	dB	-
VTX-DE-RATIO-6dB	Tx de-emphasis ratio for 5.0 GT/s	N/A	4.5 (min) 7.5 (max)	N/A	dB	-
TTX-UTJ	Tx uncorrelated total jitter	100 (max)	50 (max)	31.25 (max)	ps PP at 10-12	-
TTX-UTJ-SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	100 (max)	66.51 (max)	33.83 (max)	ps PP at 10-12	-
TTX-UDJDD	Tx uncorrelated Dj for non-embedded Refclk	100 (max)	30 (max)	12 (max)	ps PP	-
TTX-UPW-TJ	Total uncorrelated pulse width jitter	N/A	40 (max)	24 (max)	ps PP at 10-12	-
TTX-UPWDJDD	Deterministic DjDD uncorrelated pulse width jitter	N/A	40 (max)	10 (max)	ps PP	-

Symbol	Parameter Description	2.5 GT/s	5.0 GT/s	8.0 GT/s	Units	Notes
TTX-RJ	Tx Random jitter	N/A	1.4 – 3.6	1.4 – 2.2	ps RMS	Informative parameter only. Range of Rj possible with zero to maximum allowed TTX-UDJDD.
LTX-SKEW	Lane-to-Lane Output Skew	2.5 (max)	2.0 (max)	1.5 (max)	ns	Between any two Lanes within a single Transmitter.
RLTX-DIFF	Tx package plus die differential return loss	See Figure 9, page 33	See Figure 9, page 33	See Figure 9, page 33	dB	Note 6.
RLTX-CM	Tx package plus die common mode return loss	See Figure 10, page 33	See Figure 10, page 33	See Figure 10, page 33	dB	Note 6.

Notes:

1. A single combination of PLL BW and peaking is specified for 2.5 GT/s implementations. For other data rates, two combinations of PLL BW and peaking are specified to permit designers to make a tradeoff between the two parameters.

2. The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie 5 below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table. The PLL BW is defined at the point where its transfer function crosses the -3dB point.

3. Refer to Section 8.3.3.4 of the PCI Express Base Specification, Revision 4.0 for measurement details. For 8.0 GT/s and 16.0 GT/s no minimum voltage swing is specified because it is captured by VTX-BOOST-FS and VTX-BOOST-RS parameters.

4. VTX-EIEOS-FS and VTX-EIEOS-RS are measured at the device pin and include package loss. Voltage limits comprehend 10 both full swing and reduced swing modes. A Transmitter must advertise a value for LF during TS1 at 8.0 and 16.0 GT/s that ensures that these parameters are met.

5. The numbers above take into account measurement error. For some Tx package/driver combinations ps21TX may be greater than 0 dB. The channel compliance methodology at 2.5 and 5.0 GT/s assumes the 8.0 GT/s package model. 15.

6. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value.

7. The reference plane for all parameters at 2.5 and 5.0 GT/s is the package pins.

8.10.2. Common Receiver Parameters

Table 42. Common Receiver Parameters

Symbol	Parameter Description	2.5 GT/s	5.0 GT/s	8.0 GT/s	Units	Notes
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.0375 (max)	ps	UI tolerance is equivalent to ±300 ppm and does not include SSC effects.
BWRX-PKG-PLL1	Rx PLL bandwidth corresponding to PKGRX-PLL1	22 (max), 1.5 (min)	16 (max), 8 (min)	4.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function.
BWRX-PKG-PLL2	Rx PLL bandwidth corresponding to PKGRX-PLL2	Not Specified	16 (max), 5.0 (min)	5.0 (max), 2.0 (min)	MHz	Second order PLL transfer bounding function.
PKGRX-PLL1	Maximum Rx PLL peaking corresponding to BWRX-PKG-PLL1	3.0 (max)	3.0	2.0	dB	Second order PLL transfer bounding function.
PKGRX-PLL2	Maximum Rx PLL peaking corresponding to BWRX-PKG-PLL2	Not specified	1.0	1.0	dB	Second order PLL transfer bounding function.
RLRX-DIFF	Differential receiver return loss	See Figure 9, page 33	See Figure 9, page 33	See Figure 9, page 33	dB	-
RLRX-CM	Common mode receiver return loss	See Figure 10, page 33	See Figure 10, page 33	See Figure 10, page 33	dB	-
RXGND-FLOAT	Rx termination float time	500 (max)	500 (max)	500 (max)	ns	Limits added for 2.5 GT/s and 5.0 GT/s that match those for 8.0 GT/s.
VRX-CM-AC-P	Rx AC common Mode Voltage	150 (max)	150 (max)	75 (max) for EH< 100 mVPP 125 (max) for EH≥ 100 mVPP	mVP	Measured at Rx pins into a pair of 50Ω terminations to ground.
ZRX-DC	Receiver DC single ended impedance	40 (min) 60 (max)	40 (min) 60 (max)	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. For 8.0 and 16.0 GT/s is bounded by RLRX-CM. See Note 5.
ZRX-HIGH-IMP-DC-POS	DC input CM input impedance for V≥0 during Reset or power-down	≥10K (0-200 mV) ≥20K (> 200 mV)	≥10K (0-200 mV ≥20K (> 200 mV)	≥10K (0-200 mV ≥20K (> 200 mV)	Ω	Voltage measured wrt. ground. Parameters may not scale with process technology.

Symbol	Parameter Description	2.5 GT/s	5.0 GT/s	8.0 GT/s	Units	Notes
ZRX-HIGH-IMP-DC-NEG	DC input CM input impedance for V<0 during Reset or power-down	1.0K (min)	1.0K (min)	1.0K (min)	Ω	Parameters may not scale with process technology.

Notes:

1. Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in.

2. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are 5 measured during Receiver tolerancing.

3. Two combinations of PLL BW and peaking are specified at 5.0 GT/s to permit designers to make tradeoffs between the two parameters. If the PLL's min BW is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's min BW is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. Note: a PLL BW extends from zero up to the value(s) defined as the min or max in the above table. For 2.5 GT/s a single PLL 10 bandwidth and peaking value of 1.5-22 MHz and 3.0 dB are defined.

4. Measurements must be made for both common mode and differential return loss. In both cases the DUT must be powered up and DC isolated, and its D+/D- inputs must be in the low-Z state.

5. The Rx DC single ended impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance is permitted to start 15 immediately and the Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.

6. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.

7. ZRX-HIGH-IMP-DC-NEG and ZRX-HIGH-IMP-DC-POS are defined respectively for negative and positive voltages at the input of the Receiver. Transmitter designers need to comprehend the large difference between >0 and <0 Rx 20 impedances when designing Receiver detect circuits.

8. Defines the time for the Receiver's input pads to settle to new common-mode on 2.5/5.0 GT/s transition to 8.0 GT/s.

8.10.3. Tx and Rx Return Loss

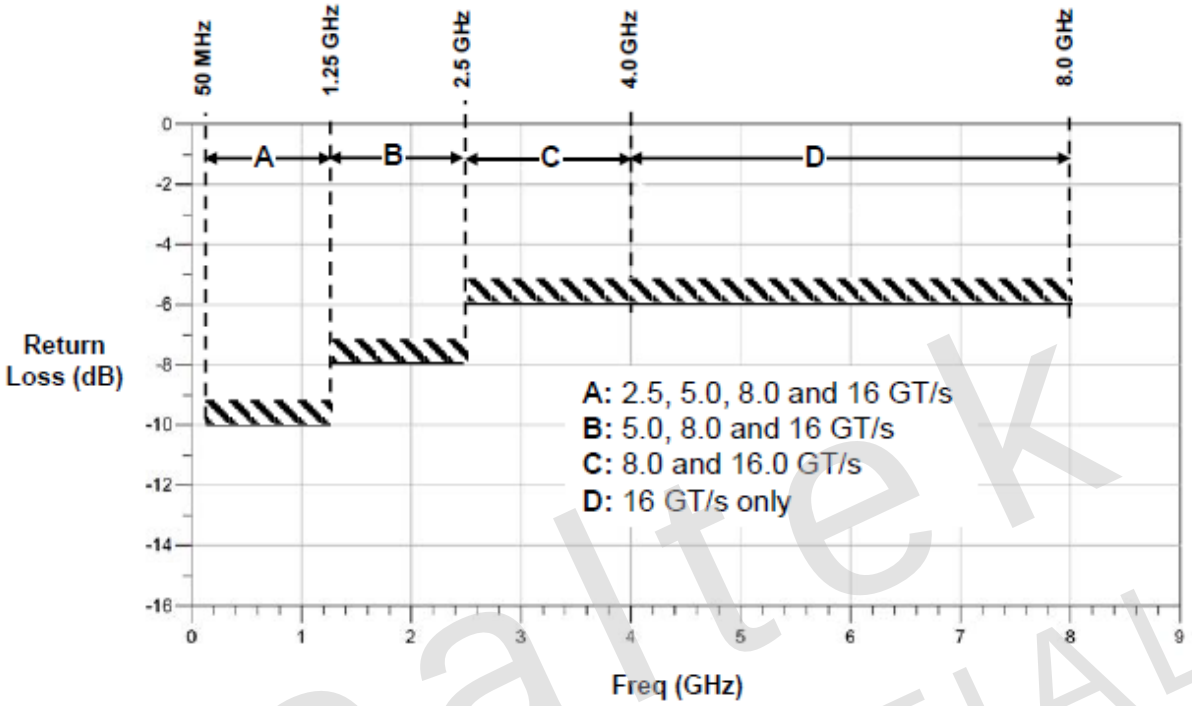


Figure 9. Tx/Rx Differential Return Loss Mask

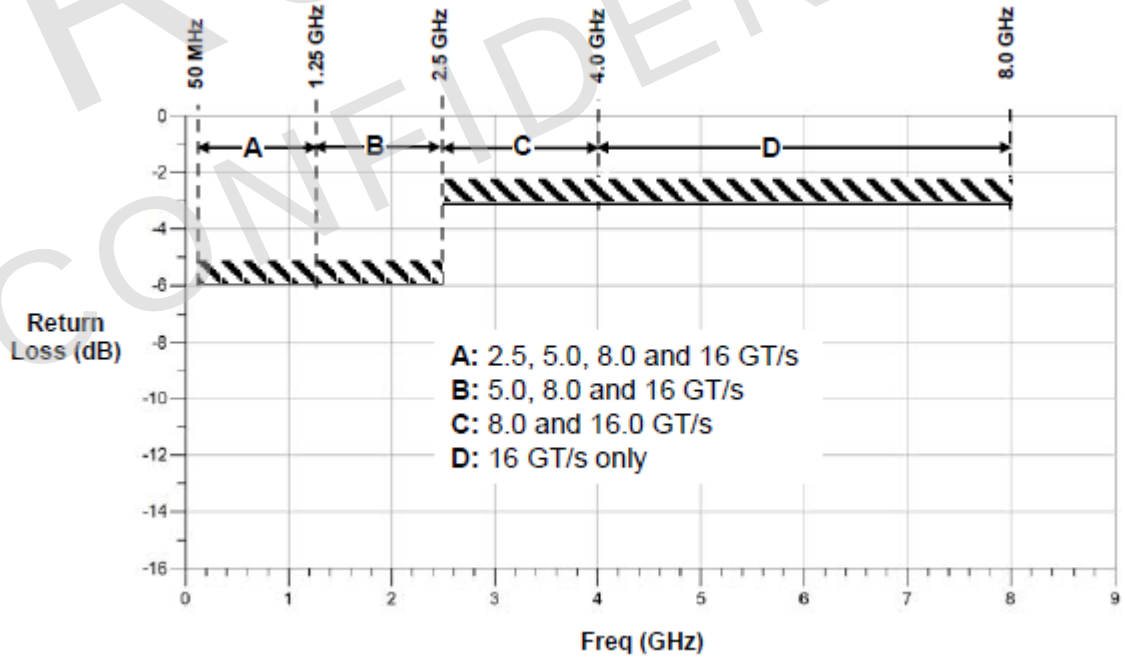


Figure 10. Tx/Rx Common Mode Return Loss Mask

8.10.4. REFCLK Parameters

Table 43. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-0.3	-	V	1, 8

Symbol	Parameter	100MHz Input Min	100MHz Input Max	Units	Note
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note 1: Measurement taken from single-ended waveform.
Note 2: Measurement taken from differential waveform.
Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 14, page 37.
Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 11, page 36.
Note 5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 11, page 36.
Note 6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 13, page 36.
Note 7: Defined as the maximum instantaneous voltage including overshoot. See Figure 11, page 36.
Note 8: Defined as the minimum instantaneous voltage including undershoot. See Figure 11, page 36.
Note 9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 11, page 36.
Note 10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.
Note 11: System board compliance measurements must use the test load card described in Figure 17, page 38. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.
Note 12: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range. See Figure 16, page 37.
*Note 13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*
Note 14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 12, page 36.
Note 15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

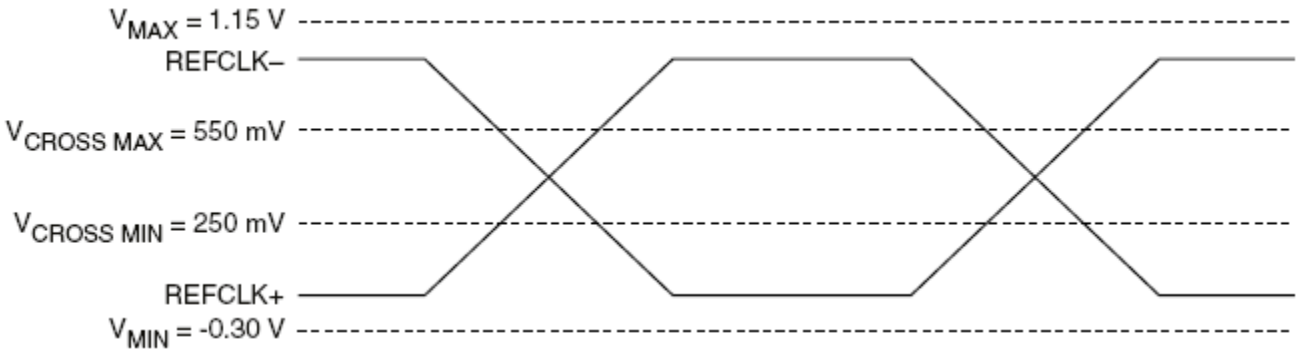


Figure 11. Single-Ended Measurement Points for Absolute Cross Point and Swing

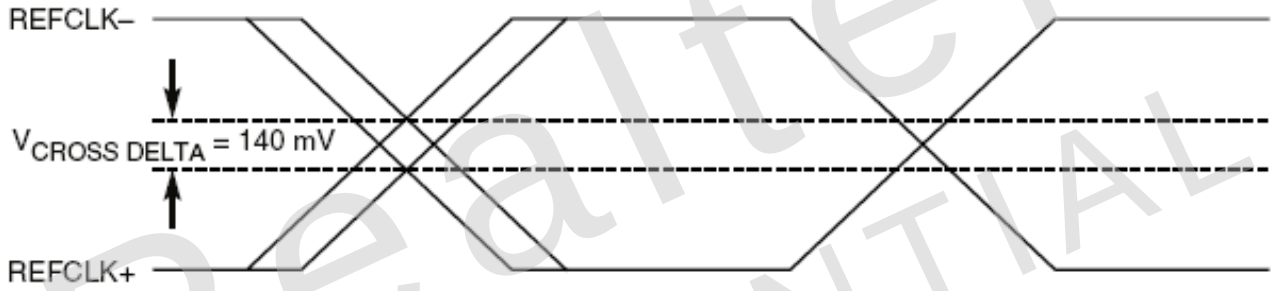


Figure 12. Single-Ended Measurement Points for Delta Cross Point

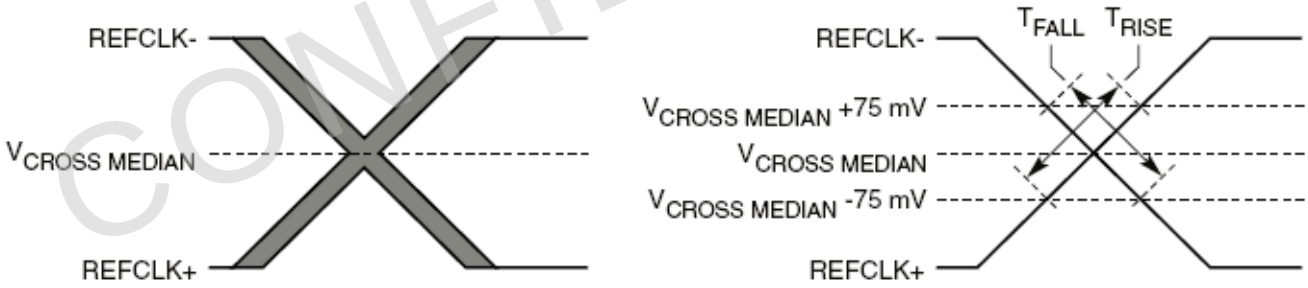


Figure 13. Single-Ended Measurement Points for Rise and Fall Time Matching

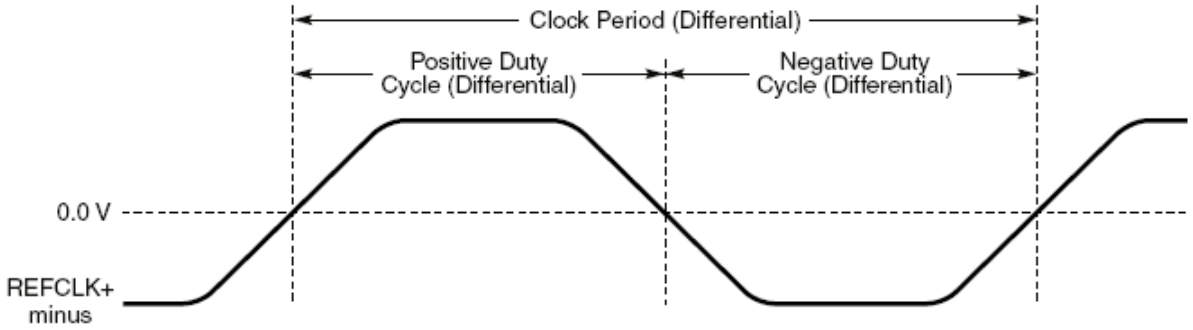


Figure 14. Differential Measurement Points for Duty Cycle and Period

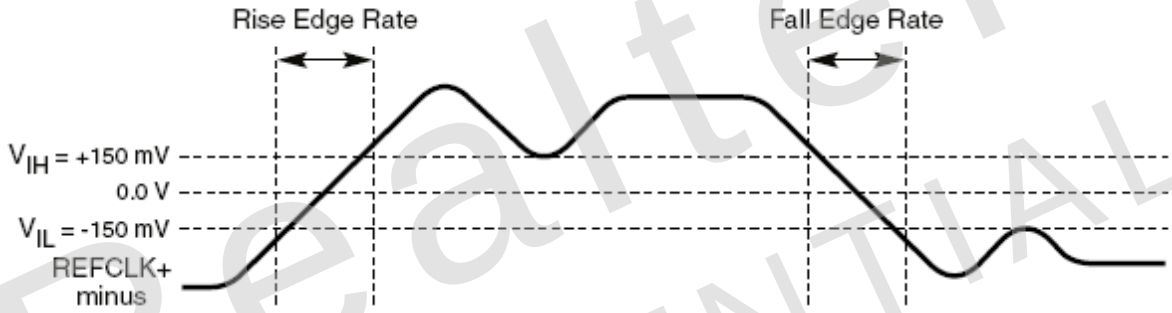


Figure 15. Differential Measurement Points for Rise and Fall Time

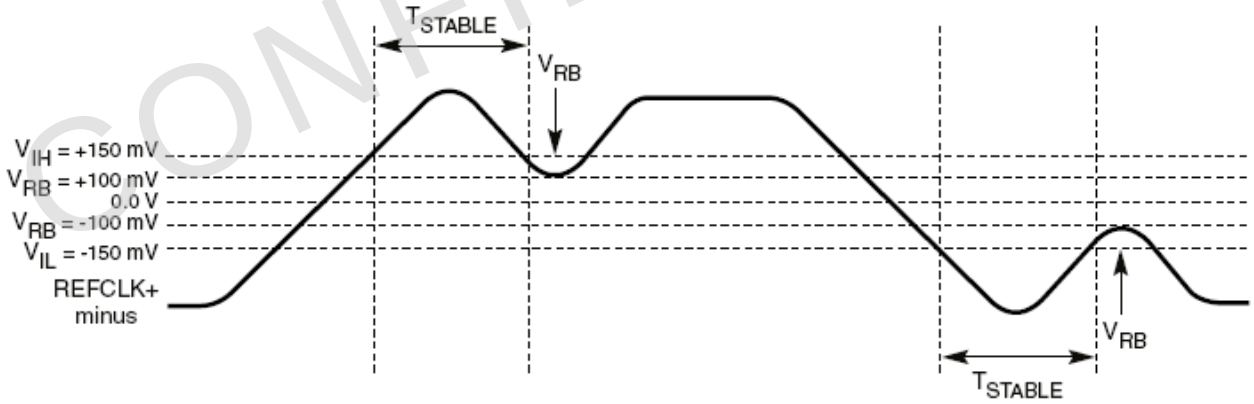


Figure 16. Differential Measurement Points for Ringback

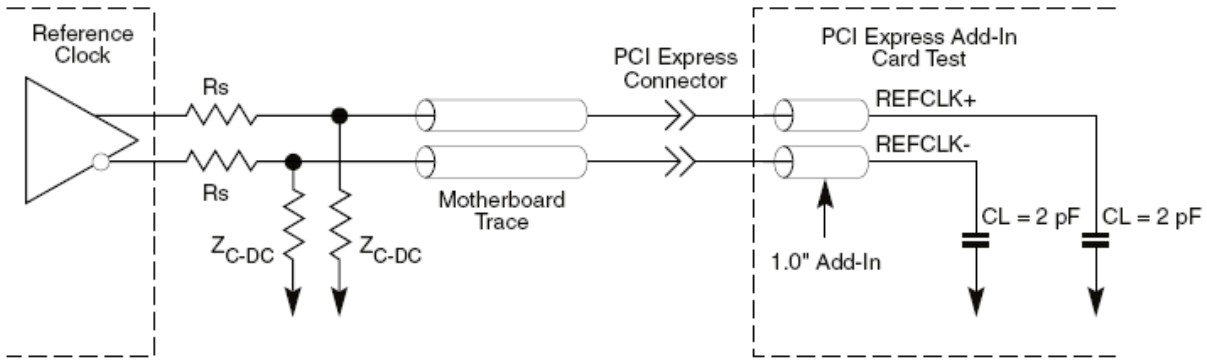


Figure 17. Reference Clock System Measurement Point and Loading

8.10.5. Auxiliary Signal Timing Parameters

Table 44. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{PERSTB-RTD}$	PERSTB Rising Time Duration	10	-	ms
T_{FAIL}*	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PWRON}	3.3Vaux Power On Time	-	-	ms

Note 1: T_{FAIL} means 500 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{FAIL} can be disregarded when implementation and timing of T_{FAIL} will not affect any LAN functions.
Note 2: 3.3V main power waveform controlled by ISOLATEBPIN.

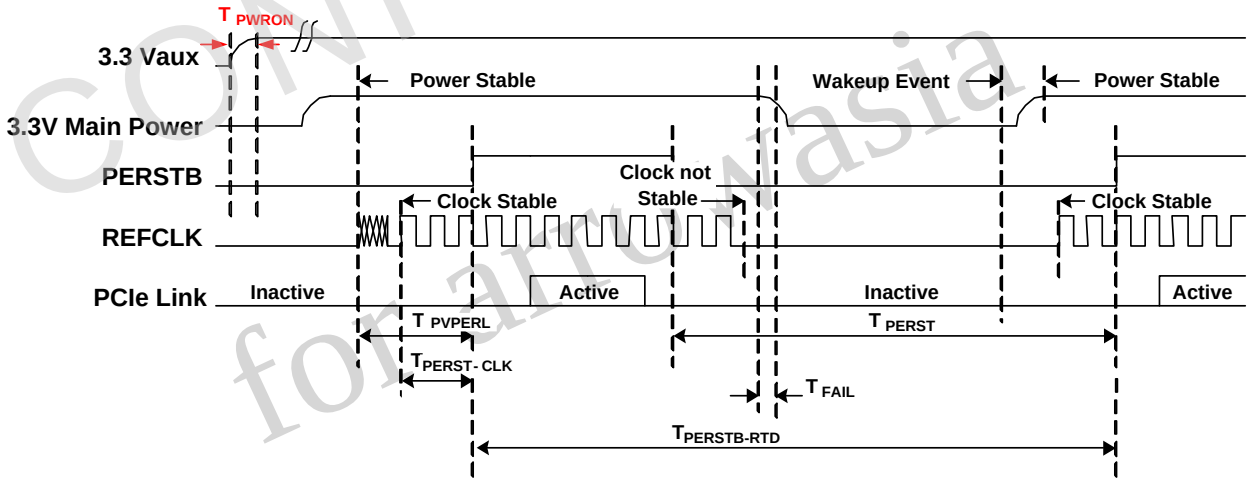


Figure 18. Auxiliary Signal Timing Parameters

9. Power Sequence

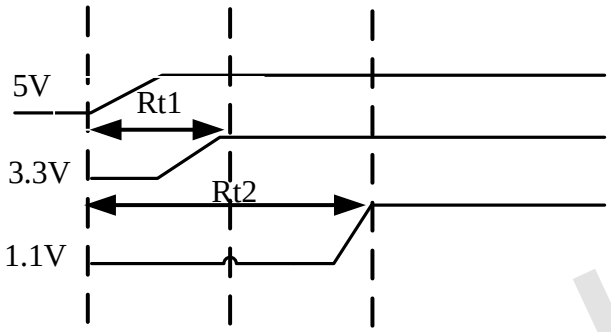


Figure 19. Power Sequence

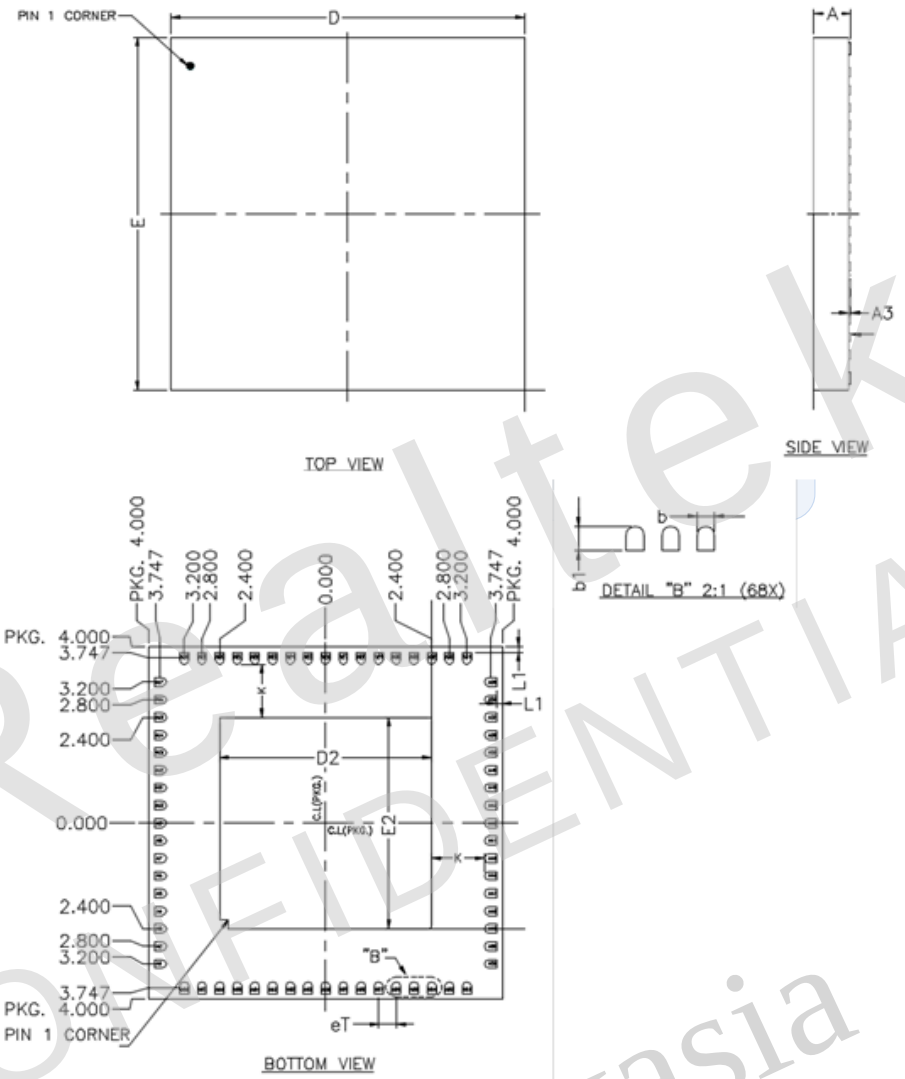
Table 45. Power Sequence Parameters

Symbol	Parameter	Min	Max	Units
Rt1	5V to 3.3V Rise Time from 0% to 100%	320	-	µs
Rt2	5V to 1.1V Rise Time from 0% to 100%	1.8	-	ms

Note 1: If a situation occurs where 5V is not fully powered down, and power comes back on in a short time period (<50ms), the RTL9210B-CG may be damaged. Please ensure this situation does not occur when testing.

10. Mechanical Dimensions

Package 68 Leads 8x8mm^2



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.85	-	-	0.033
A3	0.02	0.05	0.08	0.001	0.002	0.003
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.225	0.275	0.325	0.009	0.011	0.013
D/E	8.00 BSC			0.315 BSC		
D2/E 2	4.7	4.8	4.9	0.185	0.189	0.193
eT	0.40 BSC			0.016 BSC		
K	1.15	1.20	1.25	0.045	0.047	0.049
L1	0.075	0.125	0.175	0.003	0.005	0.007

11. Ordering Information

Table 46. Ordering Information

Part Number	Package
RTL9210B-CG	68-Pin QFN 'Green' Package

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II
Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
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